Fig 1. Non-tapered 3-input CMOS NAND gate
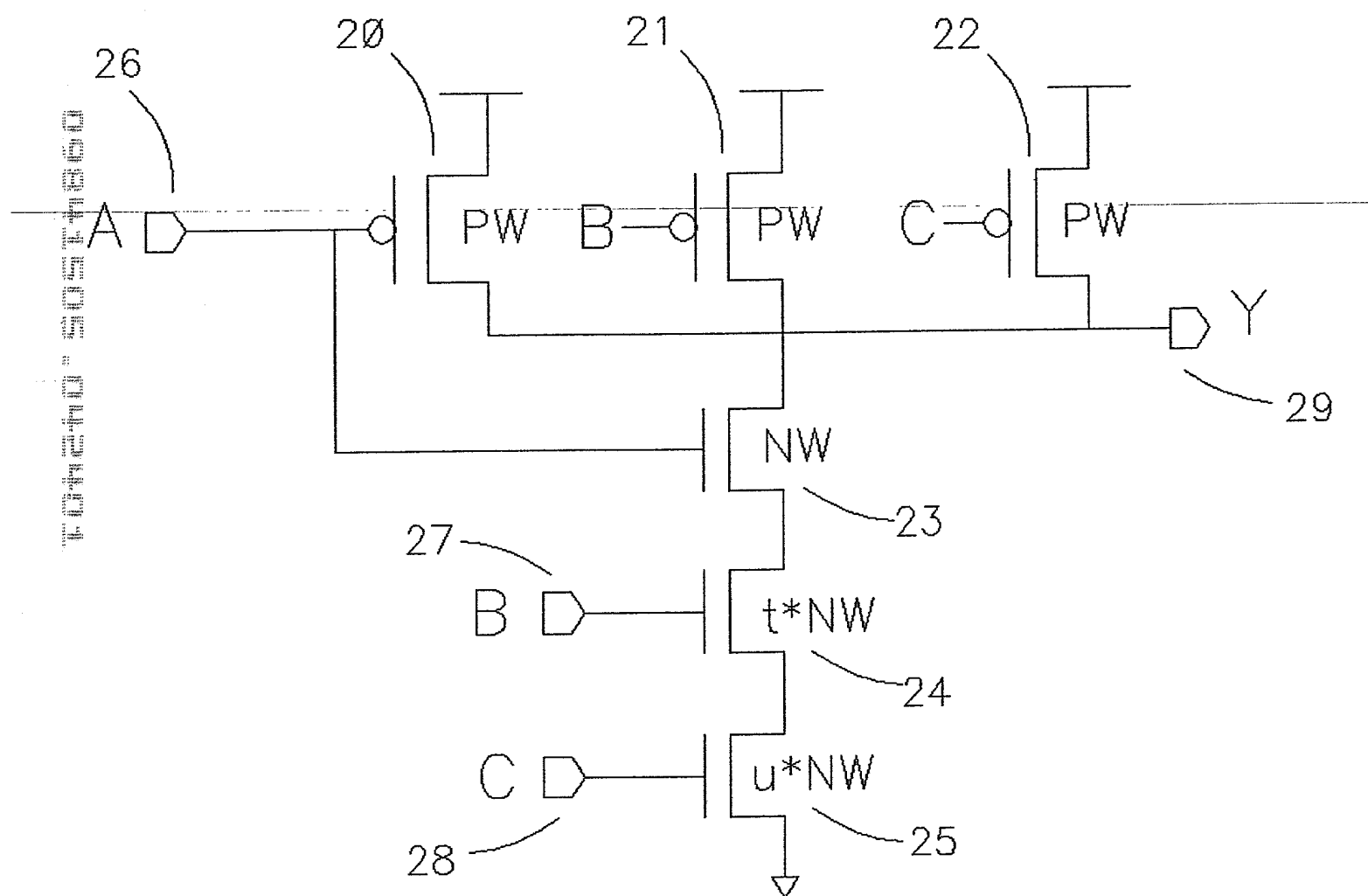
Fig 2. Tapered 3-input CMOS NAND gate
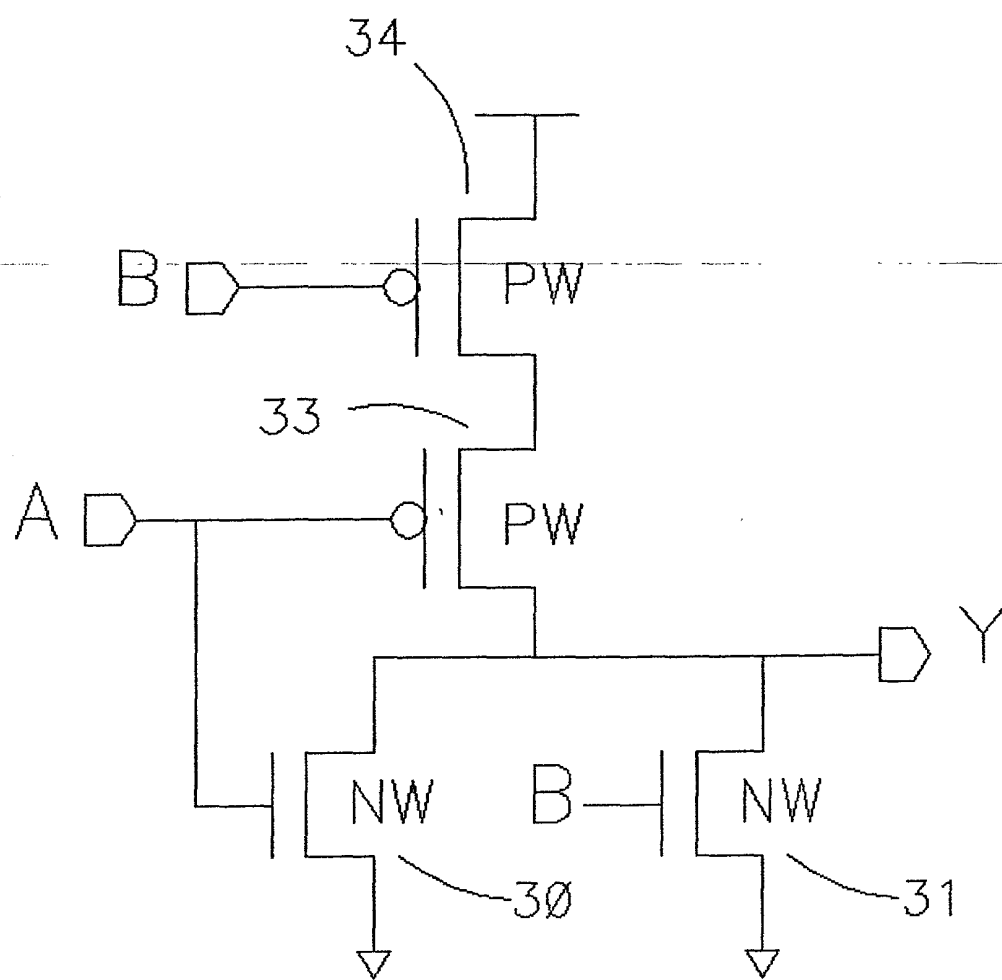
Fig 3. Non-tapered 2-input CMOS NOR gate
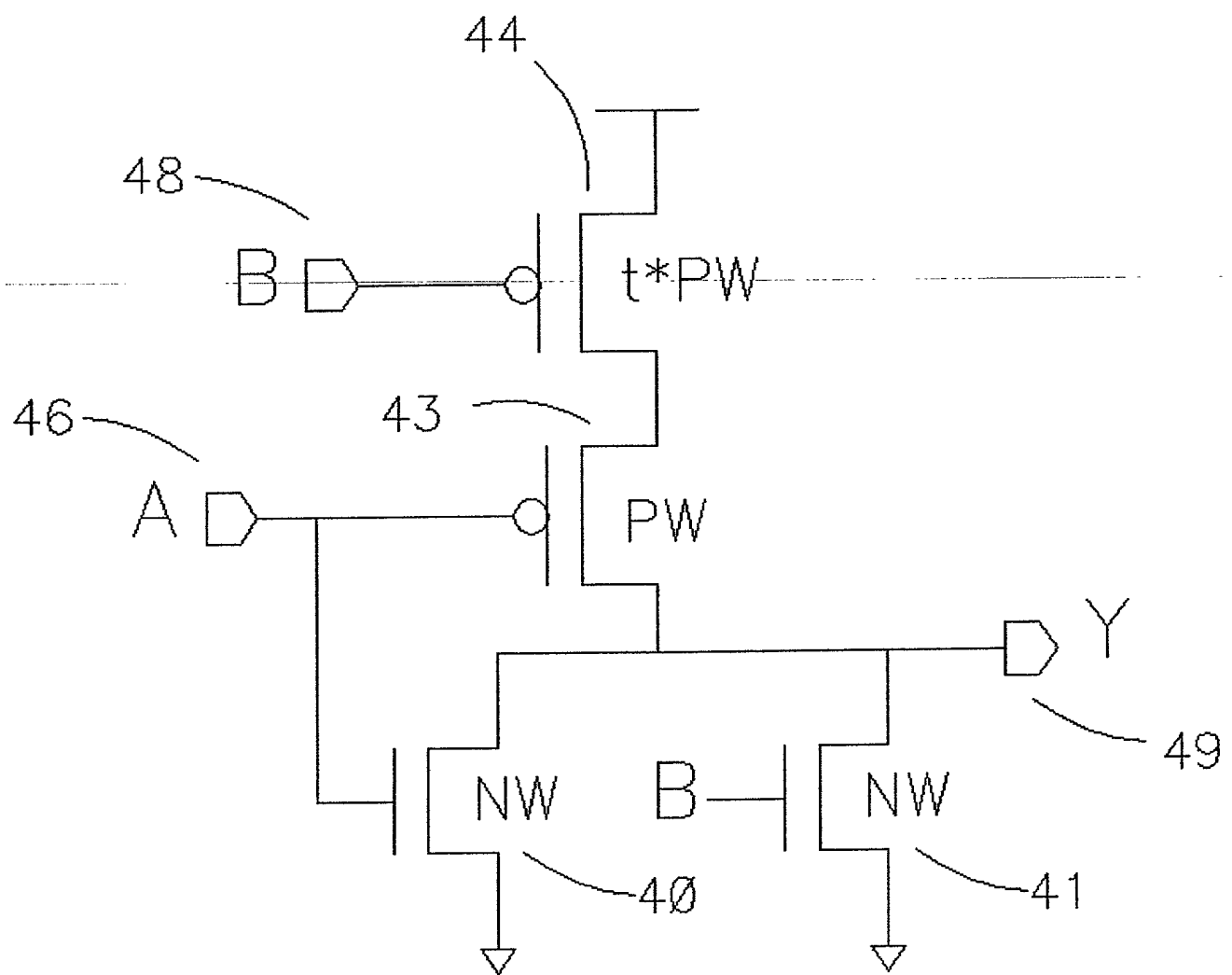
Fig 4. Tapered 2-input CMOS NOR gate

Fig. 5. 3-input NAND Path Delay
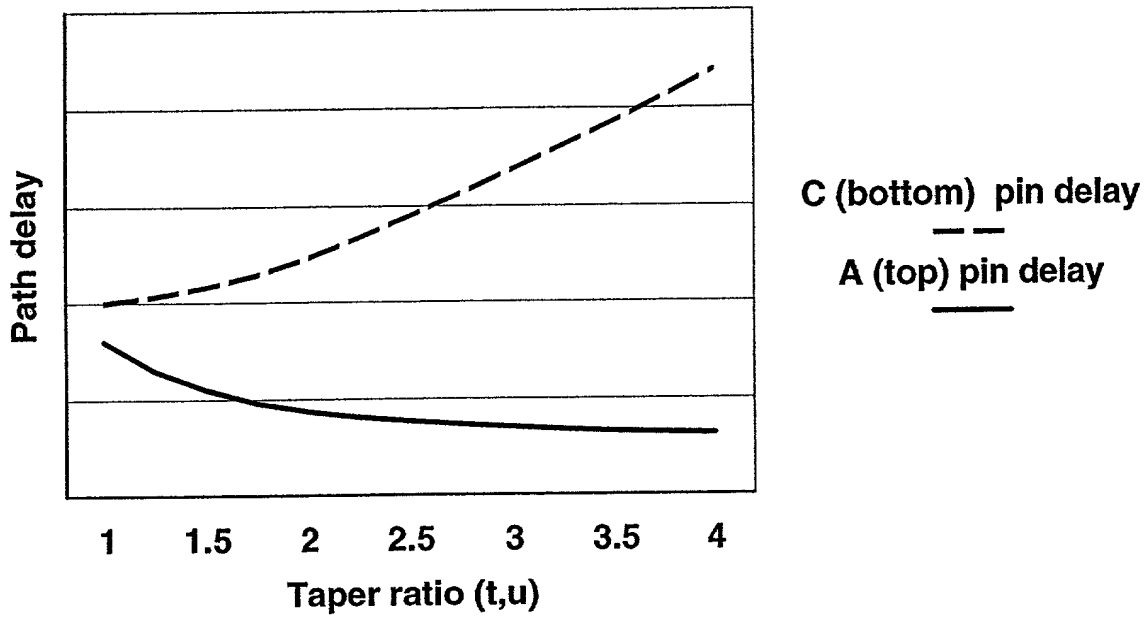## vs. Taper Ratio

C (bottom) pin delay

— —

A (top) pin delay

Start

60

Select next
timing critical
gate G

none
left

Done

61

Y   G = Inverter   N
         ?

62

N   Is most   Y
         timing critical
         net attached to
         A pin
         ?

63

Swap most—timing
critical net to
pin A

none left   Replace G with next
                 functionally—equivalent   64
                 tapered gate G'

Run timing   65
analysis

66

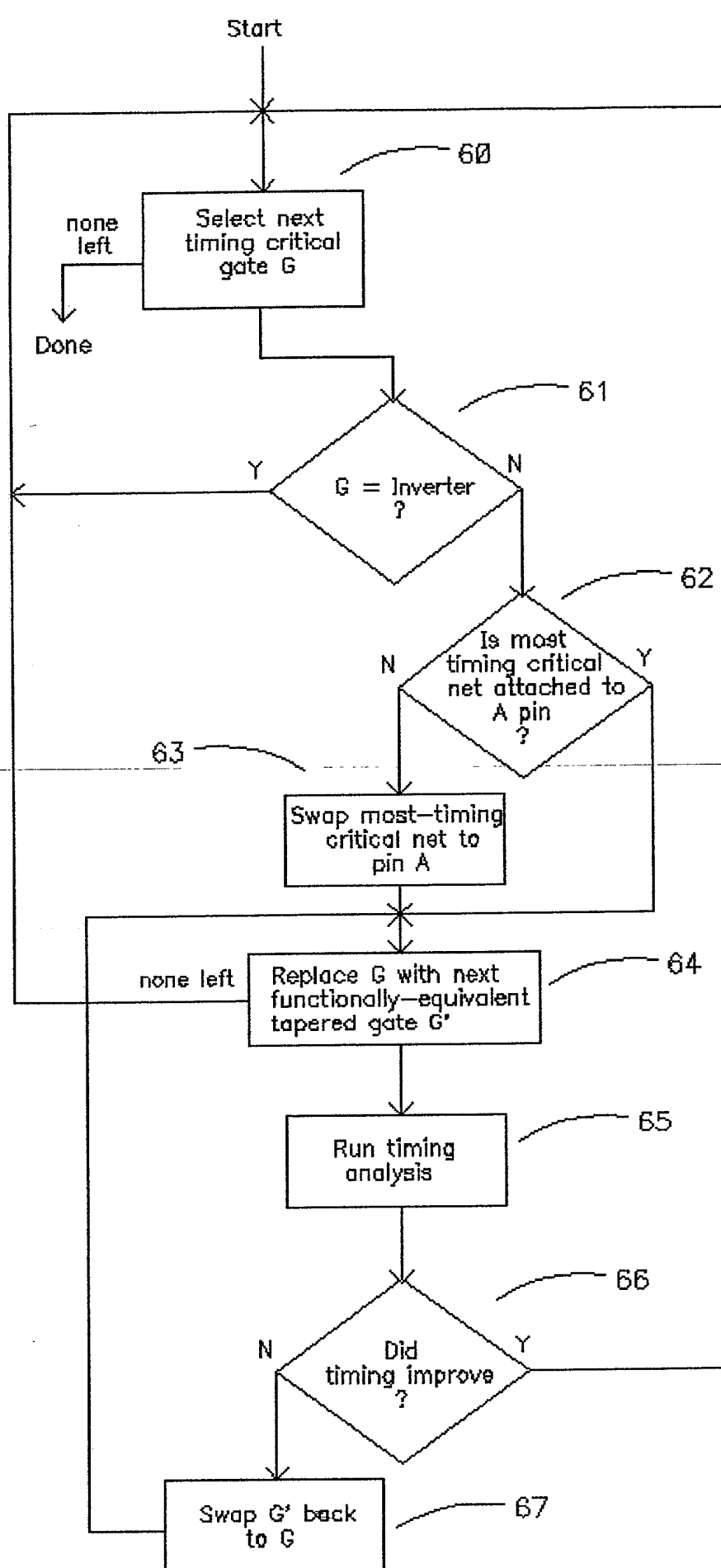N   Did   Y
         timing improve
         ?

Swap G' back   67
to G

Fig 6. Synthesis tapered algorithm